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# Low Power Delay Product(PDP), Improved Noise Margin Schmitt-Trigger Based SRAM Design, using Negative Bitline Technique

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**Abstract—***Negative bit line technique is used to improve SRAM cell performance parameters. We have added negative bit line technique to conventional Schmitt-Trigger based SRAM cell circuit to improve its parameters. It has been observed that by using negative bit line technique, write noise margin is increased by 6-8%. Moreover, Power delay product(PDP) is reduced to one-third of the conventional Schmitt-Trigger based SRAM bitcell. SRAM bitcell parameters can be further improved by applying Process Variation to this negative bit line technique circuit. The simulation has been done at 90nm technology using Silvaco (Gateway) and Microwind.*

**Index Terms***: Power Delay Product(PDP), Read Margin(RM), Write Margin(WM), Power, Delay, Negative Bit Line technique(NBL)*

## 1. INTRODUCTION

Schmitt-Trigger based SRAM bit cell incorporate a feedback mechanism .Both type of Schmitt-Trigger(ST) bitcells[1],work on a built-in feedback mechanism.First type of ST cell circuit consist of partial feedback mechanism(for 1 to 0 input transition ,feedback mechanism is not present). Second type of ST cell consists of complete feedback ie..feedback exists in both transition.

Negative Bit Line(NBL) technique is used to decrease the bit line voltage below ground(0 voltage) so that the gate to source($V_{gs}$) of access transistor is increased which increases the access ability(driving strength) of access transistors. In (NBL) technique, negative bit line voltage can be generated by using a charge pump technique or a capacitor coupling technique. The capacitor coupling technique used here involves two capacitors along with other components.

Negative Bit line Technique[2] consists of two boosting capacitors along with a generator circuit and pass transistors. Several external control signals have been used to assist whole operation of SRAM bitcell. Capacitive coupling can be used to generate a transient negative voltage at the low going bit line during write operation of SRAM cell.

Boosted bit line scheme[3] in SRAM bitcell circuit is based on charging and discharging of capacitor which occurs in two cycle. The former cycle capacitor is charged to a certain voltage and in later cycle it is used as a boost up voltage

generator.By applying process variation,[4] power dissipated through all components and area of the complete circuit can be reduced. SRAM bitcell parameters can be improved using process variation along with rearrangement of previous Schmitt Trigger[5] based SRAM bitcell circuit.

Rest of the paper is organized as follows: Section 2nd describes fundamental idea of NBL voltage generator and used driver circuit. Section 3rd explains working of proposed circuit(Schmitt Trigger cell with NBL technique circuit). Section 4th presents result analysis of proposed circuit presented in previous part(part3).In section 5th, we have described conclusion.

## 2. BASIC CIRCUIT DIAGRAMS

NBL technique(used in this paper) consists of two parts:(a)Negative bit line voltage generator,(b)Driver circuit. Both parts have been explained below:

### 2.1 NBL Voltage Generator

When Write Enable(WE) is low ie..WR is high, transistor N1 will be on ie.. point Q(or B) will be ground, so capacitor is charged to a voltage $V_{BA}$ ie..$V_{BA}$ is positive, which implies that voltage $V_{AB}$ is negative.

This negative voltage is stored in capacitor across C1.When

WE is high ie..WR becomes low,N1 will be off, so capacitor C1 retains its previous value. This negative voltage is used to lower the bit line voltage during write operation.

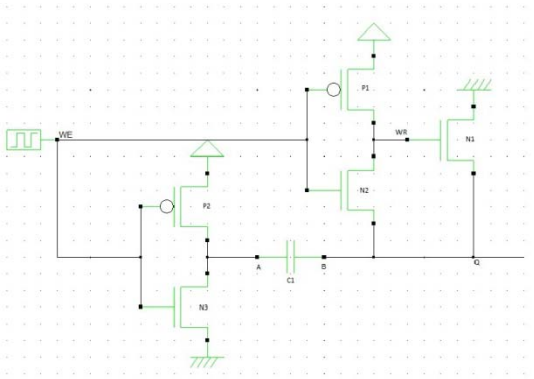


**Fig. 1: NBL voltage generator**

### Driver Circuit

When Write Enable signal is high, WR is low, depending on the status of DATA(data to be written in SRAM cell) signal, either of the transistors N1 or N1 (in figure 2) will be on and pulls the corresponding bit line to low level. When one of the bit line goes low, it disables the first set of transistors(N1 and N2) and enables second set of transistor (N3 and N4). After that, the negative voltage which is generated by Negative bit line generator, is provided to bit line BL or BR. So, the voltage of bit line is lowered below ground. Thus, driver circuit provides ease for write operation in the SRAM bitcell.

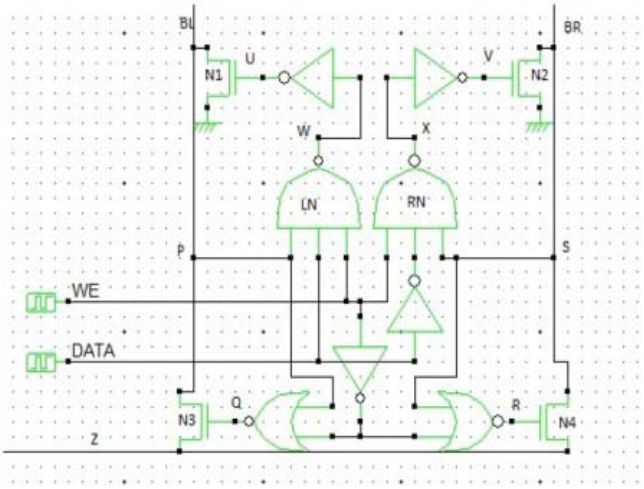


**Fig. 2: Write Driver circuit**

### 2.3 Schmitt Trigger Based SRAM bitcell

We know that schmitt Trigger bitcell works on in built feedback mechanism. Two word line (WL and WWL) are used to control read and write operation in SRAM bitcell. when both word line are high WRITE operation is performed, when WL is high and WWL is low READ operation is executed. When both word line are low SRAM bitcell is said to be in HOLD condition.

We know that Schmitt Trigger is used to vary the switching

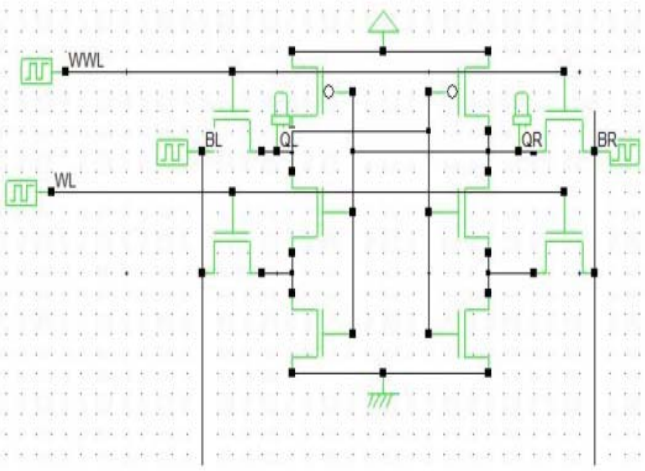


**Fig. 3: Schmitt Trigger Bitcell**

Thres hold of an inverter, depending on the direction of input transition. In Schmitt Trigger bitcell circuit, feedback mechanism is present in pull-down network only.

## 3. PROPOSED CIRCUIT (SCHMITT TRIGGER CIRCUIT WITH NBL TECHNIQUE)

In this section we are presenting Schmitt Trigger circuit along with NBL technique circuit. In the diagram presented below, there are three major parts:(a) Schmitt Trigger circuit (b) NBL voltage generator (c) Driver circuit.

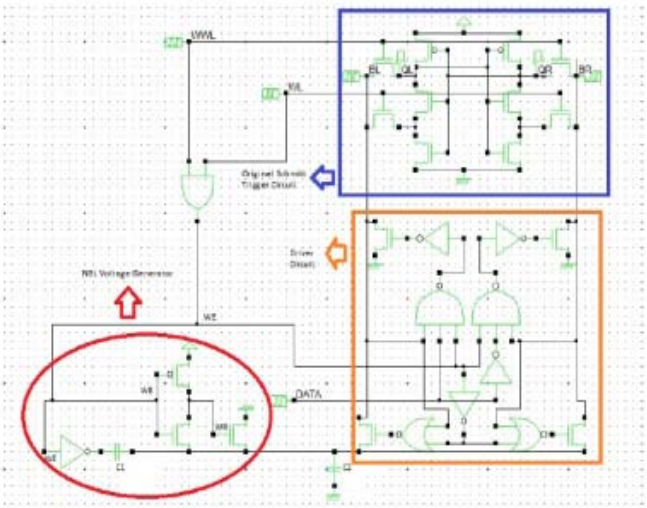


**Fig. 4: ST Bitcell With NBL Technique Circuit**

We know that in original Schmitt Trigger bitcell circuit write operation is performed when both word line (WL and WWL) are high. So, to generate a write enable (WE) with these word line,we have used an AND gate whose inputs are these word lines.Thus,it is clear that write enable(WE) will be high only if both word line(WL and WWL) are high. This generated write enable signal has been used in NBL voltage generator as well as in driver circuit. During write operation, a negative voltage is generated at the low going bit line, which increases the gate to source voltage($V_{gs}$) of access transistor, which provides ease in the write operation. So, negative bit line voltage generator along with write driver circuit increases the speed of SRAM cell.

## 4. SIMULATION RESULT AND ANALYSIS

All the simulations has been performed at room temperature 27_C. The analysis has been done using Silvaco(Gateway) and Microwind at 90nm technology.

### 4.1 Power Delay Product(PDP) calculation

Power Delay Product(PDP) is the figure of merit to determine the quality of logic circuit, also it is the measure of energy of gate. PDP is measured in Joule and define average energy consumed per switching event. If PDP is less than circuit is having good figure of merit. We also know that delay is inversely proposal to speed, so reduction in delay improves performance of SRAM cell. We know that

$$PDP = P_{avg} \_ t_{delay}$$

where Pavg = Average Power Dissipation ,tdelay =Delay time

We observed that delay in ST bitcell with NBL technique, becomes one-fourth of the original Schmitt trigger circuit. But, power has been increased in the new circuit by 20-25% compared to original Schmitt Trigger circuit. This increment in power is due to increment in number of circuit components. So, power delay product has been reduced to one third of the original ST circuit.

**Table I: Power Delay Product(PDP) of original Schmitt Trigger circuit**

| Supply(v) | Power | Delay(ps) | power delay product(aJ) |
|---|---|---|---|
| 1.0 | 21.2$\mu$W | 275 | 5830 |
| 1.2 | 36.628$\mu$W | 272 | 9962.8 |
| 1.4 | 57.385$\mu$W | 269.5 | 15465.3 |
| 1.6 | 84.203$\mu$W | 268 | 22566.4 |
| 1.8 | 0.118mW | 267 | 31506 |

**Table II: Power Delay Product(PDP) ST Cell with NBL Technique Circuit(Proposed Circuit)**

| Supply(v) | Power | Delay(ps) | Power Delay Product(aJ) |
|---|---|---|---|
| 1.0 | 28.136$\mu$W | 63 | 1772.6 |
| 1.2 | 47.771$\mu$W | 62 | 2961 |
| 1.4 | 73.814$\mu$W | 61 | 4502.65 |
| 1.6 | 0.107mW | 60.5 | 6473.5 |
| 1.8 | 0.148mW | 60.5 | 8954 |

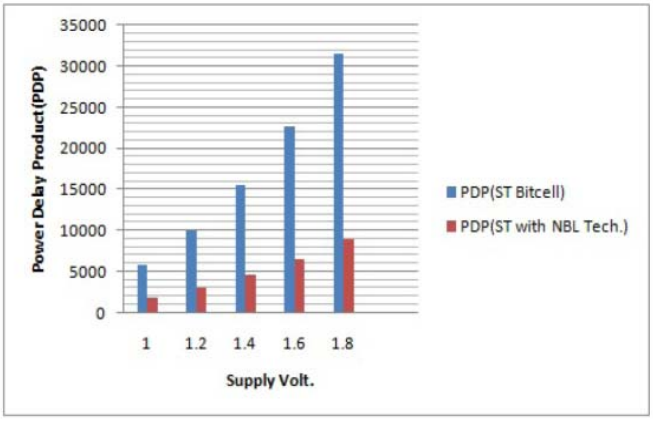


**Fig. 5: Power Delay Product Comparison**

### 4.2 Noise Margin Measurement

We observed that using NBL technique to the previous Schmitt Trigger circuit, write noise margin increases. It can be seen that noise margin increases as supply voltage increases, but this increment occurs upto a limit only, ie.. noise margin starts decreasing after a certain limit.

**Table III: Comparison of Write Noise Margin of Proposed Circuit (NBL Circuit) to Original Schmitt Trigger CIRCUIT**

| Supply Volt. | WM(ST Bitcell) | WM(ST with NBL Tech.) |
|---|---|---|
| 1.2 | 0.3528 | 0.37311 |
| 1.4 | 0.38015 | 0.4043 |
| 1.6 | 0.40173 | 0.42177 |
| 1.8 | 0.4221 | 0.43934 |

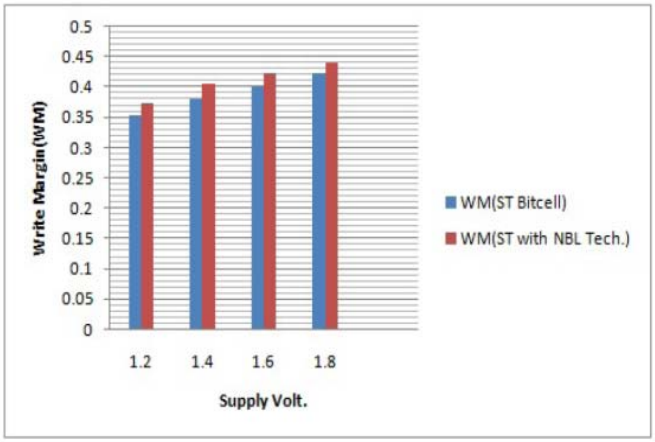


**Fig. 6: Noise Margin Comparison**

Noise margin also depends on driver to access transistor aspect ratio.Noise margin increases when this aspect ratio is increased,and this improvement in noise margin reaches to a saturation value when this aspect ratio is 2:1 ie.. no improvement is observed after 2:1 ratio.

## 5. CONCLUSION AND FUTURE WORK

This work shows that using NBL Technique in the previous Schmitt Trigger bitcell circuit, power delay product reduces to a great extent. Write noise margin also improves when NBL technique circuit is added to original Schmitt Trigger circuit. The SRAM bitcell parameters can be further improved by applying other read-write assist techniques to this new circuit. Process variation will also be helpful to get desired improvement in present SRAM circuit parameters. The properties of SRAM bitcell can be enhanced to a great extent by applying a combination of more than one read-write assist techniques

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